1. A method of fabricating a semiconductor wafer, comprising:

providing a generally planar semiconductor wafer substrate such that said substrate is defined by substantially orthogonal first and second in-plane dimensions;

defining a topographic layer of conductive lead line material such that said topographic layer projects onto said substrate to occupy at least a portion of said substantially orthogonal first and second in-plane dimensions;

depositing at least one said topographic layer of conductive lead line material on said substrate;

depositing a plurality of topographic fill patterns adjacent either said topographic layer of conductive lead line material or another of said plurality of topographic fill patterns such that spaces defined therebetween possess substantially equal width as any other space;

arranging said plurality of topographic fill patterns and said at least one said topographic layer of conductive lead line material so that a grid defined by a plurality of crossings of said spaces contains no linear dimension longer than the longest dimension of any one of said plurality of topographic fill patterns, and that no intersection defined by any of said plurality of crossings includes uninterrupted linear dimensions; and

depositing a planarization layer over said substrate such that it is disposed at least within said grid and laterally surrounds said at least one topographic layer of conductive lead line material and said plurality of topographic fill patterns.

2. A method according to claim 1, wherein said step of depositing a planarization layer includes depositing a layer of spin-on glass.

3. A method according to claim 1, wherein said step of depositing a planarization layer includes directly applying TEOS by chemical vapor deposition.

4. A method according to claim 1, whereupon deposition of said planarization layer produces a top surface of said layer substantially co-planar with a top surface of said topographic layer of conductive lead line material and said plurality of topographic fill patterns.

5. A method according to claim 1, comprising the additional step of defining an array comprising at least one of said plurality of topographic fill patterns and topographic layers such that no portion of any of said plurality of topographic layers overhangs a boundary of said array.

6. A method according to claim 5, wherein the additional step of defining said array further includes defining said array boundary mostly with straight edges of said plurality of topographic fill patterns.

7. A method of fabricating a semiconductor device, comprising:

providing a semiconductor substrate;

depositing at least one topographic layer of conductive lead line material on said substrate;

depositing a plurality of topographic fill patterns adjacent either said topographic layer of conductive lead line material or another of said plurality of topographic fill patterns such that spaces defined therebetween possess substantially equal width as any other space;

arranging said plurality of topographic fill patterns and said at least one said topographic layer of conductive lead line material so that an array defining a plurality of valleys forms over said substrate and circumscribes at least one of said topographic fill patterns and said conductive lead line material, said array configured such that a periphery thereof is substantially bounded by straight edges of said plurality of topographic fill patterns, said conductive lead line material, or a combination of both, said array further configured such that no portion of any of said topographic fill patterns extends laterally beyond said periphery, and such that said topographic fill patterns and said conductive lead line material comprise a grid defined by a plurality of crossings of said spaces, said grid disposed within said array and containing no linear dimension longer than the longest dimension of any one of said plurality of topographic fill patterns, and that no intersection defined by any of said plurality of crossings includes uninterrupted linear dimensions; and

depositing a planarization layer over said substrate such that it is disposed at least within said grid and laterally surrounds said at least one topographic layer of conductive lead line material and said plurality of topographic fill patterns.